



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,080	10/06/2003	Kouji Okamoto	60188-671	4066
7590 Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY 600 Thirteenth Street, N.W. Washington, DC 20005-3096			EXAMINER ADEGEYE, OLUWASEUN	
			ART UNIT 2621	PAPER NUMBER
			MAIL DATE 03/20/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/678,080

**Applicant(s)**

OKAMOTO ET AL.

**Examiner**

OLUWASEUN A. ADEGEYE

**Art Unit**

2621

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10/06/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 - 15 is/are pending in the application.
- 4a) Of the above claim(s) 6 and 11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 5, 7 - 10 and 12 - 15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10/06/2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/S508)
- Paper No(s)/Mail Date 11/02/2008
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

2. The references listed on the information disclosure statement filed on 10/06/2003 and 11/02/2006 have been considered by the examiner (see attached PTO – 1449).

### ***Claim Objections***

3. Claims 7 – 10 and 12 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 2, 5, 7- 10 and 12 are rejected under 35 U.S.C. 102(b) based upon a public use or sale of the invention. Okazaki (US 6,003,051).

As to **claim 1**, Okazaki discloses a reproduction signal processing device, comprising:

an A/D converter (10) for quantizing an input analog reproduction signal (output from 9) into digital reproduction signal data (digital data) (see column 8, lines 11 – 16);

an adaptive equalizer (16) for equalizing the reproduction signal data (digital data) with a characteristic controlled according to data input to the adaptive equalizer and data output from the adaptive equalizer (see column 8, lines 44 – 54)); and

a PLL circuit (15) for outputting a clock signal which is in synchronization with the reproduction signal data (see column 8, lines 38 – 43);

an analog filter (9) for removing noise from the reproduction signal (see column 8, lines 1 – 7); and

a digital filter (11) provided between the A/D converter and the adaptive equalizer, the digital filter equalizing the reproduction signal data with a fixed characteristic (see column 8, lines 17 – 24, column 9, lines 38 – 40 and column 10, lines 50 – 56),

a control section (20) for determining the fixed characteristic of the digital filter during a learning period and setting, after the learning period, the characteristic of the digital filter by synthesizing the characteristic of the digital filter with a characteristic of the adaptive equalizer converged by the operation of the adaptive equalizer (see column 8, line 65 - column 9, line 10, column 10, line 50 - column 11, line 2),

wherein the PLL circuit (15) outputs the clock signal based on an output of the digital filter (see column 4, lines 28 – 31).

As to **claim 2**, Okazaki discloses a reproduction signal-processing device according to claim 1, wherein the analog filter has a low pass characteristic (see column 8, lines 1 – 7).

As to **claim 5**, Okazaki discloses a reproduction signal processing device according to claim 1, wherein the digital filter is a FIR filter (see column 8, lines 17 – 23) which has a characteristic determined according to one or more tap coefficients set in the digital filter (see column 8, lines 17 – 24, column 9, lines 38 – 40, column 10, lines 50 – 56 and column 12, lines 39 - 48).

As to **claim 7**, Okazaki discloses a reproduction signal processing device according to claim 6, wherein:

the digital filter is a FIR filter which has a characteristic determined according to one or more tap coefficients set in the digital filter(see column 8, lines 17 – 24, column 9, lines 38 – 40, column 10, lines 50 – 56 and column 12, lines 39 - 48) and

the control section sets any of a plurality of tap coefficient candidate values in the digital filter, thereby determining the fixed characteristic of the digital filter (see column 10, line 50 – column 11, line 35).

As to **claim 8**, Okazaki discloses a reproduction signal processing device according to claim 6, wherein the control section determines the fixed characteristic of the digital filter based on a value corresponding to a phase error in the PLL circuit (see column 1, lines 48 – 65).

As to **claim 9**, Okazaki discloses a reproduction signal processing device according to claim 6, wherein the control section determines the fixed characteristic of

Art Unit: 2621

the digital filter based on an equalization error in the adaptive equalizer (see column 10, lines 17 – 23 and column 10, lines 42 – 56).

As to **claim 10**, Okazaki discloses a reproduction signal processing device according to claim 6, wherein the control section determines the fixed characteristic of the digital filter based on a difference between data input to the adaptive equalizer and data output from the adaptive equalizer (see column 10, lines 17 – 23 and column 10, lines 42 – 56).

As to **claim 12**, Okazaki discloses a reproduction signal processing device according to claim 11, wherein:

each of the digital filter and the adaptive equalizer includes a FIR filter which has a characteristic determined according to one or more tap coefficients(see column 8, lines 17 – 24, column 9, lines 38 – 40, column 10, lines 50 – 56 and column 12, lines 39 - 48); and

the control section sets, as the tap coefficient in the digital filter, a value obtained by the sum-of-products operation of the tap coefficient determined such that the digital filter has the predetermined characteristic and the tap coefficient determined such that the adaptive equalizer has the converged characteristic (see column 11, lines 3 – 35 and column 12, lines 49 – 58).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazaki in view of Shigenobu (6,072,756).

As to **claim 13**, Okazaki discloses a reproduction signal processing device according to claim 1, wherein the PLL circuit outputs a first clock signal for driving the adaptive equalizer and a second clock signal for driving the A/D converter and the digital filter (see column 8, lines 38 – 43).

Okazaki does not disclose the second clock signal having a frequency that is N times higher than that of the first clock signal where N is an integer equal to or greater than 2.

Shigenobu discloses the second clock signal having a frequency that is N times higher than that of the first clock signal where N is an integer equal to or greater than 2 (see column 10, lines 30 – 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set frequency of the second clock signal to be N times larger than that of the first clock signal where N is a integer equal to or greater than 2 as taught by Shigenobu to the apparatus of Okazaki to provide an optical disk apparatus and a data recording method which can easily generate a clock signal for a data process and a clock signal for a physical address reproducing process (see column 1, lines 42 – 45).

7. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazaki in view of Yamada et al (US 7,227,963 B1).

As to **claim 3**, Okazaki discloses a reproduction signal processing device according to claim 1 but does not disclose wherein the digital filter has a high band emphasis characteristic.

Yamada discloses wherein the digital filter has a high band emphasis characteristic (see column 7, lines 31 – 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have added a digital filter has a high band emphasis characteristic as taught by Yamada to the apparatus of Okazaki to provide a signal processing apparatus having an improved operability (see column 1, lines 38 – 42)

As to **claim 4**, Yamada discloses a reproduction signal processing device according to claim 3, wherein the digital filter has a low pass characteristic which allows the passage of a lower frequency component as compared with the analog filter (see column 7, lines 31 – 36).

8. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazaki in view of Okubo (US 6,157,603).

As to **claim 14**, Okazaki discloses a reproduction signal processing device according to claim 1, wherein:

the reproduction signal processing device reads recorded data from a recording medium (see column 7, line 28 – 31);

the analog filter has a low pass characteristic (see column 8, line 1 – 7); and



Okazaki discloses adjusting the upper limit of the frequency component of the analog filter (see column 8, lines 6 – 9) but he does not disclose the upper limit of a frequency component which is allowed to pass through the analog filter is changed according to the speed of reading the recorded data.

Okubo discloses the upper limit of a frequency component which is allowed to pass through the analog filter is changed according to the speed of reading the recorded data (see column 6, lines 23 – 59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have added changing the upper limit of the analog filter according to the speed of reading the recorded data as taught by Okubo to the apparatus of Okazaki to provide a reproduction apparatus in which the frequency of the clock signal used is made to follow its reproduction rate (see column 2, line 66 – column 3, line 4).

As to **claim 15**, Okazaki discloses a reproduction signal processing device according to claim 1, wherein:

the reproduction signal processing device reads recorded data from a recording medium(see column 7, line 28 – 31);

the PLL circuit outputs a first clock signal for driving the adaptive equalizer and a second clock signal for driving the A/D converter and the digital filter (see column 8, lines 38 – 43);

Okubo discloses the frequency of the first clock signal is determined according to the speed of reading the recorded data (see column 6, lines 23 – 59); and

the frequency of the second clock signal is substantially constant irrespective of the speed of reading the recorded data (see column 6, lines 23 – 59).

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,671,112 discloses A/D converter, phase locked loops and filters.

### ***Inquiries***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to OLUWASEUN A. ADEGEYE whose telephone number is (571)270-1711. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on 571-272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2621

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

03/13/2008

/O.A/

/Marsha D. Banks-Harold/  
Supervisory Patent Examiner, Art Unit 2621